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IN THE CLAIMS

Please amend claims 1 and 5 to read as follows:

1. (Twice Amended) A hard macro having an antenna rule violation free input/output port, comprising:

- B1
- an input/output (I/O) port having a port level metallic conductor in a low level metalization layer;
 - an I/O transistor having a gate conductor separated from a diffusion region by a gate oxide layer;
 - a top level metallic conductor of a highest level metalization layer that is electrically coupled to a diffusion region; and
 - an electrical connection between the port level metallic conductor and the gate conductor including a first conducting section extending from the gate conductor to the top level metallic conductor and a second conducting section extending from the top level metallic conductor to the port level conductor;

wherein the I/O port is free of antenna rule violations, and the I/O port, the I/O transmitter, the top level metallic conductor, and the electrical connection form a predefined circuit element that is droppable into a floor plan of a circuit design.

5. (Amended) A method of defining a hard macro having an antenna rule violation free input/output port, comprising steps of:

- B2
- (a) defining an input/output (I/O) port having a port level conductor in a low level metalization layer;
 - (b) defining an I/O transistor having a gate conductor separated from a diffusion region by a gate oxide layer;

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- B2
- (c) defining a top level metallic conductor in a highest level metalization layer that is electrically coupled to a diffusion region;
 - (d) defining a first conducting section of an electrical connection extending from the gate conductor to the top level metallic conductor; and
 - (e) defining a second conducting section of the electrical connection extending from the top level metallic conductor to the port level conductor;

wherein the defined I/O port is free of antenna rule violations, and the defined I/O port, transistor, top level metallic conductor, and the electrical connection form a predefined circuit element that is droppable into a floor plan of a circuit design.
